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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,666	10/22/2003	Eiji Aoki	4074-7	6492

23117 7590 06/08/2005

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EXAMINER	
ROSASCO, STEPHEN D	
ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,666	AOKI ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohnuma (6,370,441) or Tounai et al. (2002/0043615).

The claimed invention is directed to a photomask defect testing method, a photomask manufacturing method and a semiconductor integrated circuit manufacturing method. In the photomask defect testing method, reference data is created from corrected photomask design data that is corrected on the basis of an exposure transfer pattern, and sensor data is created by measuring the shape of the photomask based on the corrected photomask design data. Furthermore, first non-testing region data indicating non-testing regions including pattern portions having a predetermined width or less and pattern spaces having a predetermined value or less is extracted from the corrected photomask design data, the extracted first non-testing region data is stored so as to be included in the corrected photomask design data, the non-testing regions indicated by the first non-testing region data is excluded, and the reference data is compared with the sensor data, whereby defects on the photomask are detected.

And wherein said photomask design data includes beforehand second non-testing region data indicating non-testing regions including pattern portions having a predetermined width or less and pattern spaces having a predetermined value or less; and said first step further comprises a step of finally creating non-testing region data by ORing said first non-testing region data with said second non-testing region data.

And wherein said predetermined width and said predetermined value are the minimum value detectable at said fourth step.

Ohnuma teaches a method of optical exposure comprising the step of exposing a photo resist formed on a substrate through a photomask with exposure light to transfer a pattern formed in the photomask to the photo resist formed on the substrate, said photomask obtained by the fabricating steps of;

correcting designed-pattern data obtained by data-processing a plurality of designed patterns, preparing pattern data for electron beam exposure from the corrected designed-pattern data, exposing an electron beam resist formed on a mask blank with an electron beam on the basis of the obtained pattern data for electron beam exposure, forming an etching mask by developing the electron beam resist, and etching the mask blank with the etching mask, wherein the correction of the designed-pattern data comprises the steps of;

(a) producing hierarchical-area-bitmapped bitmap data from a plurality of the designed-pattern data,

(b) determining a line width of the designed pattern and a space width between said designed pattern and a designed pattern adjacent to said designed pattern, from said hierarchical-area-bitmapped bitmap data, and

(c) correcting the designed-pattern data on the basis of the determined line width and the determined space width, for proximity effect correction and/or optical proximity effect correction.

Ohnuma also teaches a method of fabricating a semiconductor device comprising the steps of exposing a photo resist formed on a substrate through a photomask with exposure light to transfer a pattern formed in the photomask to the photo resist formed on the substrate,

developing the photo resist to obtain an etching mask, and etching the substrate with the etching mask, said photomask obtained by the method above.

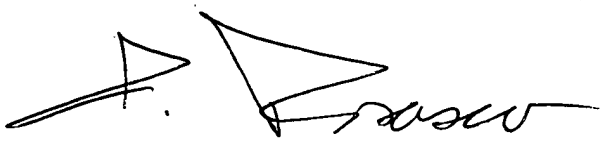
Tounai et al. teach an optical proximity effect correcting method in a semiconductor manufacturing process, comprising: adding a first correcting region around a portion of a first design pattern, said portion facing a second design pattern, and a first corrected design pattern including said first correcting region and said first design pattern; detecting a space between said first corrected design pattern and said second design pattern; judging whether said space is smaller than or equal to a predetermined value; and deleting at least a portion of said first correcting region such that said space is larger than said predetermined value, when said space is smaller than or equal to said predetermined value.

Tounai et al. also teach a mask data forming method in a semiconductor manufacturing process, comprising: adding a correcting region to a design pattern based on a first data indicating at least a portion of said design pattern to form a first corrected pattern; and correcting said correcting region of said first corrected pattern based on a second data different from said first data to form a second corrected pattern; generating a mask data based on said second corrected pattern, and wherein said correcting includes deleting at least a portion of said correcting region such that a space between said correcting region and one of another design pattern and another first corrected pattern is not smaller than a predetermined value.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
6/1/05